PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Docket No: Q77597
Yasushi KINOSHITA	
Appln. No.: 10/669,655	Group Art Unit: 2811
Confirmation No.: 5578	Examiner: Samuel A. GEBREMARIAM
Filed: September 25, 2003	

For: SEMICONDUCTOR INTEGRATED CIRCUIT

SUPPLEMENTAL AMENDMENT UNDER 37 C.F.R. § 1.116

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Further to the Amendment filed September 24, 2007, please amend the above-identified application as follows on the accompanying pages.

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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A semiconductor integrated circuit comprising:

a power supply wiring;

a ground wiring; and

a decoupling capacitor formed between said power supply wiring and said ground wiring, said decoupling capacitor comprising an upper electrode, a lower electrode, and an insulating material in between the electrodes,

wherein at least one of the electrodes of said decoupling capacitor comprises a shield layer formed in a plane shape on a semiconductor substrate, and said shield layer is electrically connected directly to said semiconductor substrate via a diffusion layer, and extends from the diffusion layer to the decoupling capacitor in a plane parallel to the substrate, such that a plane shaped portion of said shield layer contacts said diffusion layer, said shield layer is fixed to a power supply potential or said ground potential, and said decoupling capacitor does not overlap said diffusion layer,

and wherein the lower electrode comprises the shield layer.

2. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein, another of the electrodes of said decoupling capacitor, which opposes the electrode comprising said shield layer, includes a wiring layer connected to wirings on an uppermost layer of a multilayer wiring structure via contact electrodes, and a capacitor insulating film for forming said decoupling capacitor is provided between said wiring layer and said shield layer.

3. (currently amended): A semiconductor integrated circuit comprising:

a power supply wiring;

a ground wiring; and

a decoupling circuit formed between said power supply wiring and said ground wiring, said decoupling circuit comprising an upper electrode, a lower electrode, and an insulating material in between the electrodes,

wherein at least one electrode of said decoupling circuit comprises a shield layer obtained by covering a plurality of protrusions formed on a semiconductor substrate, and said shield layer is electrically connected directly to the semiconductor substrate via a diffusion layer, and extends from the diffusion layer to the decoupling capacitor in a plane parallel to the substrate, such that a plane shaped portion of said shield layer contacts said diffusion layer, said shield layer is fixed to a power supply potential or said ground potential, and said decoupling circuit does not overlap said diffusion layer, and

wherein the lower electrode comprises the shield layer.

4. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said protrusions are formed simultaneously with a gate electrode by a same formation process used for the gate electrode.

5. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein said decoupling capacitor is formed on an element isolation oxide film.

6. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein said shield layer comprises a silicon compound of a metal.

7. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said decoupling circuit is formed on an element isolation oxide film.

8. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said shield layer comprises a silicon compound of a metal.

9. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein said diffusion layer is a well contact diffusion layer.

10. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said diffusion layer is a well contact diffusion layer.

11. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein said semiconductor substrate includes a p-well region and an n-well region.

12. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said semiconductor substrate includes a p-well region and an n-well region.

13. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein said decoupling capacitor is located opposite side with reference to a near gate electrode formed on said semiconductor substrate.

14. (currently amended): A semiconductor integrated circuit comprising:

a power supply wiring;

a ground wiring; and

a decoupling capacitor formed between said power supply wiring and said ground wiring, said decoupling capacitor comprising an upper electrode, a lower electrode, and an insulating material in between the electrodes,

wherein at least one of electrodes of said decoupling capacitor comprises a shield layer formed in a plane shape on a semiconductor substrate, and said shield layer is electrically connected directly to said semiconductor substrate via a diffusion layer, and extends from the diffusion layer to the decoupling capacitor in a plane parallel to the substrate, such that a plane shaped portion of said shield layer contacts said diffusion layer and is a lowermost conductive layer on said semiconductor substrate, said shield layer is fixed to a power supply potential or said ground potential, and said decoupling capacitor does not overlap said diffusion layer and is located adjacent to said diffusion layer, and

wherein the lower electrode comprises the shield layer.

15. (previously presented): The semiconductor integrated circuit as claimed in claim 14, wherein, another of said the electrodes of said decoupling capacitor, which opposes said electrode comprising said shield layer, includes a wiring layer connected to wirings on an uppermost layer of a multilayer wiring structure via contact electrodes, and a capacitor insulating film for forming said decoupling capacitor is provided between said wiring layer and said shield layer.

16. (previously presented): The semiconductor integrated circuit as claimed in claim 14, wherein said decoupling capacitor is formed on an element isolation oxide film.

17. (previously presented): The semiconductor integrated circuit as claimed in claim 14, wherein said shield layer comprises a silicon compound of a metal.

18. (previously presented): The semiconductor integrated circuit as claimed in claim 14, wherein said diffusion layer is a well contact diffusion layer.

19. (previously presented): The semiconductor integrated circuit as claimed in claim 14, wherein said semiconductor substrate includes a p-well region and an n-well region.

20. (canceled).

21. (canceled).

REMARKS

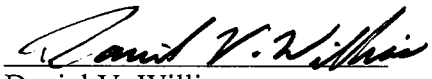
Claims 1-19 are pending. By this Amendment, Applicant amends claims 1, 3 and 14, and cancels claims 20 and 21. Applicant presumes that the Amendment filed September 24, 2007 has been entered and is incorporated herein. Thus, in the above shown amendments, only the changes that are being presently made are shown with markings.

Applicant thanks the Examiner for contacting us on October 29, 2007 regarding a proposed amendment to the independent claims. Specifically, the Examiner suggested incorporating the features recited in dependent claims 20 and 21 respectively to independent claims 1 and 3. Independent claim 14 is also similarly amended. The Examiner indicated that this amendment would overcome the applied art. Applicant amends the claims as suggested by the Examiner.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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